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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/788,560	Applicant(s) Yamazaki et al.
	Examiner ORI NADAV	Group Art Unit 2811

☒ Responsive to communication(s) filed on *Nov 28, 2000* .

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *78-157* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *78-157* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on 11/28/2000. These drawings are approved by the examiner.

Specification

2. Claims 78, 90 and 126 are objected to because of the following informalities: The phrase "one ore more elements" should read "one or more elements". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 78, 80, 84, 86 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. (4,755,865).

Wilson et al. teaches in figure 3 substantially the entire claimed structure, including a MOS transistor comprising a silicon semiconductor layer 42 comprising a channel region 42B in between source and drain regions 42A, a gate electrode 44 adjacent the channel region with gate insulating film 43 interposed therebetween, and a region 42C formed in the semiconductor layer containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E15 atoms per cm cube or more (column 4, lines 39-49), wherein the region is formed in the vicinity of a boundary region between the channel region and one of the source and drain regions, and wherein the channel region containing boron (column 6, lines 31-32).

Wilson et al. do not explicitly disclose a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm cube. However, Wilson et al. teach diffusing impurities at concentration of from 10E15 to 5X10E17 atoms per cm cube (column 6, lines 36-37), and under certain processing conditions the channel region can have similar concentration (column 6, lines 64-66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm in Wilson et al.'s device, since adjusting the amount of impurity concentration in a semiconductor device is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 84, the claimed limitations of a region having higher energy band gap than any of the source, drain and channel regions is inherent in Wilson et al.'s device, because a region having elements selected from a group consisting of carbon, nitrogen and oxygen, has higher energy band gap than a region containing boron.

5. Claims 78-101, 110-115, 117-127, 129-138 and 146-157 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. (4,755,865) in view of Saito et al. (4,772,927) and Shizukuishi et al. (4,841,348).

Wilson et al. teaches in figure 3 substantially the entire claimed structure, as above, except a display device having a plurality of pixels and at least one driver circuit for driving the pixels.

A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). In this case, using a MOS transistor in a CMOS device, and using the CMOS device as a driver, stagger, inverted stagger, planar and inverted planar type transistors in a peripheral circuit of an active matrix display device having plurality of pixels is a

recitation of the intended use of a structure which does not add to the structural limitations in the body of the claim

Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Therefore, the claimed structure is considered to be in at least obvious over the Wilson et al.'s structure.

In the alternative, Saito et al. teach a MOS transistor in figure 1e comprising a semiconductor film comprising crystalline silicon (column 1, lines 19-20) and a channel region 7 in between source and drain regions 6, a gate electrode 9 adjacent the channel region with gate insulating film 5 interposed therebetween, wherein the source and drain regions have at least one portion containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E19 atoms per cm cube or more (column 3, line 49 to column 4, line 24), formed in a CMOS device (figure 2).

Shizukuishi et al. teach a MOS transistor being used in a CMOS device which is part of a peripheral circuit of an active matrix type device having plurality of pixels

(abstract), and formed of a semiconductor film comprising amorphous silicon (column 3, line 48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Wilson et al.'s transistor in a CMOS device which is part of a peripheral circuit of an active matrix type device having plurality of pixels, because it is conventional in the art to connect individual transistors in order to form a CMOS device, and it is well known in the art to use CMOS transistors as drivers in a peripheral circuit of an active matrix type device having plurality of pixels. The combination is motivated by the teachings of Saito et al. who point out the advantages of using a TFT transistor having source and drain regions containing carbon, nitrogen or oxygen at a concentration higher than 10E19 atoms per cm cube or more in a CMOS device.

Regarding claims 78, 89-90, 101, 110-111, 118-119, 126-127, 146-147 and 152-153, although Wilson et al. do not explicitly disclose a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm cube, Wilson et al. teach diffusing impurities at concentration of from 10E15 to 5X10E17 atoms per cm cube (column 6, lines 36-37), and under certain processing conditions the channel region can have similar concentration (column 6, lines 64-66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a channel region containing impurities at a concentration of from 10E15 to 5X10E17

atoms per cm in Wilson et al.'s device, since adjusting the amount of impurity concentration in a semiconductor device is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization. Saito et al. teach a channel region having at least one portion containing one or more elements selected from a group consisting of carbon, nitrogen and oxygen at a concentration higher than 10E19 atoms per cm cube or more (column 5, lines 20-23).

Regarding claims 83, 95, 125, 133, the claimed limitations of an element concentration in the channel region being lower than that of the element in the region is inherent in Wilson et al.'s device, because the concentration of a region naturally tends to be higher at the center and lower at the periphery of the region.

6. Claim 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al. and Shizukuishi et al., as applied above, and further in view of Solheim (5,219,784).

Wilson et al. and Saito et al. teach substantially the entire claimed structure, as above, except a threshold voltage of an NMOS being approximately equivalent to that of the PMOS.

Solheim teaches a threshold voltage of an NMOS being approximately equivalent to that of the PMOS (column 4, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use of a threshold voltage of an NMOS being approximately equivalent to that of the PMOS in Wilson et al. and Saito et al.'s device, since adjusting the threshold voltage is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization, depending on the intended use of the device.

7. Claims 128 and 139 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. and Saito et al., as applied to claims 102, 110, 118, 126 above, and further in view of Higashi et al. (4,694,317).

Wilson et al. and Saito et al. teach substantially the entire claimed structure, including a first interlayer insulating film (ILD) 10 (Saito et al.) comprising inorganic material, and a gate electrode comprising a silicon film containing phosphorus (Wilson et al., column 3, lines 38-40, and column 6, line 32). Wilson et al. and Saito et al. do not teach a second ILD film comprising organic resin and a pixel electrode on the second ILD film formed in a transparent or a reflective device.

Higashi et al. teach in figure 1D a transparent or a reflective device comprising a first interlayer insulating film 5 comprising inorganic material, a second ILD film 7 comprising organic resin and a pixel electrode 11 on the second ILD film (column 3, line 64 to column 4, line 48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second ILD film comprising organic resin under a pixel electrode in Wilson et al.'s device, in order to provide better protection for the device. The combination is motivated by the teachings of Higashi et al. who point out the advantages of using an organic ILD film under a pixel electrode in a TFT transistor.

8. Claims 102-107, 109 and 140-144 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al. and Shizukuishi et al., as applied above, and further in view of Ovshinsky et al. (4,766,471).

Wilson et al., Saito et al. and Shizukuishi et al. teach substantially the entire claimed structure, as applied above, except an element comprising carbon.

Ovshinsky et al. teach elements selected from a group consisting of carbon, nitrogen and oxygen, can widen the band gap in silicon layer containing elements such as germanium or boron. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an element comprising carbon in Wilson et al., Saito et al. and Shizukuishi et al.'s device, in order to widen the energy band gap of the device. Note that substitution of materials is not patentable even when the substitution is new and useful. Safetran Systems Corp. v. Federal Sign & Signal Corp. (DC NIII, 1981) 215 USPQ 979.

Regarding claim 105, although Wilson et al. do not explicitly disclose a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm cube, Wilson et al. teach diffusing impurities at concentration of from 10E15 to 5X10E17 atoms per cm cube (column 6, lines 36-37), and under certain processing conditions the channel region can have similar concentration (column 6, lines 64-66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a channel region containing impurities at a concentration of from 10E15 to 5X10E17 atoms per cm in Wilson et al.'s device, since adjusting the amount of impurity concentration in a semiconductor device is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

9. Claim 145 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., as applied above, and further in view of Higashi et al. (4,694,317).

Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al. teach substantially the entire claimed structure, including a first interlayer insulating film (ILD) 10 (Saito et al.) comprising inorganic material, and a gate electrode comprising a silicon film containing phosphorus (Wilson et al., column 3, lines 38-40, and column 6, line 32). Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al. do not teach a second ILD film

comprising organic resin and a pixel electrode on the second ILD film formed in a transparent or a reflective device.

Higashi et al. teach in figure 1D a transparent or a reflective device comprising a first interlayer insulating film 5 comprising inorganic material, a second ILD film 7 comprising organic resin and a pixel electrode 11 on the second ILD film (column 3, line 64 to column 4, line 48).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second ILD film comprising organic resin under a pixel electrode in the device of Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., in order to provide better protection for the device. The combination is motivated by the teachings of Higashi et al. who point out the advantages of using an organic ILD film under a pixel electrode in a TFT transistor.

10. Claim 108 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., as applied above, and further in view of Solheim (5,219,784).

Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al. teach substantially the entire claimed structure, as above, except a threshold voltage of an NMOS being approximately equivalent to that of the PMOS.

Solheim teaches a threshold voltage of an NMOS being approximately equivalent to that of the PMOS (column 4, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use of a threshold voltage of an NMOS being approximately equivalent to that of the PMOS in the device of Wilson et al., Saito et al., Shizukuishi et al. and Ovshinsky et al., since adjusting the threshold voltage is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization, depending on the intended use of the device.

Response to Arguments

11. Applicant argues on page 22 that Wilson et al. do not teach regions containing oxygen or nitrogen located in source or drain regions.

The claimed limitations of a region being formed in the vicinity of a boundary region between the channel region and one of the source and drain regions, do not include the limitations of a region being located in the source or drain regions. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

12. Applicant argues on page 22 that prior art does not teach a device used as a display device.

A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*,In this case, the semiconductor device taught by prior art can very well be used as a CMOS transistor in a display device.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

William Mintel

William Mintel
Primary Examiner
Art Unit 2811

Ori Nadav, Ph.D.

January 9, 2001